REMARKS

The examiner rejected claim 1 as being directed to non-statutory subject matter. The examiner stated in part:

> **Claim 1 is rejected under 35 U.S.C. 101 because the step of directing the branch in execution of an instruction stream based on the specified value being true or false and including the token specifying the number of instructions before branch could be represented by symbols in a flowchart by pencil on a paper. Although the claim recites "execution of an instruction", it does not require the use of hardware. For example, it could be represented by a branch of an instruction symbol in a flow chart diagram based on the true or false labels or token label determination on a paper. ...**

Applicant has amended claim 1 to recite executing a branch instruction in execution of an instruction stream in the processor. As amended, claim 1 clearly requires the use of hardware.

The examiner rejected claims 1-9, 11-13, 1 5, 17, 19-21 under 35 U.S.C. 102(a) and (b) as being anticipated by Hasegawa (5,724,563).

The examiner stated:

> **As to the newly amended feature of claim 1, the change of "a branch instruction that causes" to " directing a branch instruction" does not affect the original scope of the claim. Hasegawa's branch instruction also directed a branch (see the branch flow in col.3, lines 25-30, lines 55-59, col.9, lines 29-33, col.12, lines 37-46, see fig.5B, fig. 10B).**

In addition, in reply to applicant's arguments the examiner stated:

> **As to a) above, Hasegawa did disclose a directing of a branch (see the branch instruction IBranch) that caused a branch in execution of an instruction stream (instruction at the target address and the sequence) based on any specified value being true or false: and including a token that specified number of instructions in an instruction stream that were after the branch instruction (see the instructions following the Branch) to execute before the branch operation (see the number of successive instructions designated by the predictive branch before the branch control flow was changed in col.3, lines 25-30, lines 55-59, col.9, lines 29-33, col.12, lines 37- 46, see figs., 10B Branch after 3 to X , Branch after 3 to X, Branch after 4 to X, see the decision on branch condition in col-1, lines 19-22 for the background teaching of true or false, see also col.1 1 , lines 14-24, col.12, lines 6-13 for judging a branch condition).**

Claim 1, as amended, is distinct over Hasegawa. Claim 1 recites executing a branch instruction in execution of an instruction stream with a branch based on a specified value being true or false and including a first token that specifies the number of instructions in the instruction stream that are after the branch instruction to execute before performing the branch operation and a second token that specifies a branch guess operation.

Hasegawa neither describes nor suggests the combination of a branch instruction including a first token that specifies the number of instructions in the instruction stream that are after the branch instruction to execute before performing the branch operation and a second token that specifies a branch guess operation.

Hasegawa discloses a branch instruction format that includes a region for storing 21, a region for specifying a branch target address 22 and region for storing the number of instructions to branch point 23. (see FIG. 2) Hasegawa does not disclose, suggest or even mention the combination of a first token that specifies the number of instructions after the branch instruction to execute before performing the branch operation and a second token that specifies a branch guess operation. Accordingly, claim 1 is not anticipated by Hasegawa.

Claim 2 further distinguishes by reciting that the second token that specifies the branch guess operation if set, pre-fetches a guessed instruction. Hasegawa does not suggest such a feature.

Claim 3 further distinguishes by reciting that the branch instruction further comprises an optional token that indicates a pipeline stage that the branch operation is evaluated in. Hasegawa does not suggest such a feature.

Claims 4-9 and 11-13 are allowable at least for the reasons discussed in claim 1.

Applicant canceled claims 15-16.

Claim 17 recites "executing a branch instruction that causes a branch operation in an instruction stream based on any specified value being true or false." Hasegawa neither describes nor suggests executing a branch instruction that causes a branch operation in an instruction stream based on *any* specified value being true or false. Accordingly, claim 17 is not anticipated by Hasegawa.

The examiner uses Hasegawa and Khim Yeoh to reject claim 10 as having been obvious. Claim 10 is not obvious in view of Hasegawa and Khim Yeoh. Claim 10 recites that the branch instruction causes the processor to branch to the instruction at a specified label if a specified byte in a longword matches or mismatches a byte_compare_value

Khim Yeah discloses an improved register-based I/O microcontroller that does not teach or suggest directing a branch in execution of an instruction stream based on any specified value being true or false. Khim Yeah only tests bits in a single flag register that reflect an ALU status but fails to teach or suggest testing within an instruction:

> A flag register 35 is conventionally connected to receive bits that show the status of the ALU operations, for example a bit to show an overflow in the ALU when an add instruction is executed. Other instructions test these bits and for example perform conditional operations such as a branch after an operation to compare the bytes in registers A and B. (col. 3, lines 12-18)

One skilled in this art would not be motivated to combine Hasegawa and Kim because such a combination merely adds an ALU status indicator to a region for storing, a region for specifying a branch target address and region for storing the number of instructions to branch point. No combination of Hasegawa and Khim Yeoh yields a branch instruction with the features of claim 10. Accordingly, claim 10 is not obvious in view of Hasegawa and Khim Yeoh.

The examiner uses Hasegawa and Bruckert to reject claims 14, 16 and 18 as having been obvious.

These claims are allowable at least for the reasons given for claim 1.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this

paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Enclosed is a **$150** check for excess claim fees. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 8/4/03

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